Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A data transfer method in which scanning lines in a row direction and signal lines in a column direction are formed in a matrix pattern, and a data signal which corresponds to a position on the matrix is applied within one horizontal period to a signal line which corresponds to this position, the signal lines being divided into a plurality of blocks and being sequentially conducted for each line per block so as to transfer the data signal between a matrix section and a data transfer section with respect to each block, the method comprising the step ~~of~~,of:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, ~~respectively:~~ respectively,

conducting the SL2 as preliminary conduction within one horizontal period prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

Claim 2 (currently amended): A data transfer method for an image display device having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and displaying an image according to a data signal by a pixel on the matrix, the method applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, and the data signal being transferred per block from a data transfer section to the pixel by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, the method comprising the step ~~of~~,of:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, ~~respectively:~~ respectively,

inverting a polarity of a potential of the SL2 as preliminary conduction with respect to the reference voltage within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

Claim 3 (original): The method as set forth in claim 1, wherein the signal lines of the plurality of blocks are simultaneously conducted within said one horizontal period prior to the time the application of the data signal to the BL1 is finished.

Claim 4 (original): The method as set forth in claim 1, wherein, during the preliminary conduction of the BL2, the signal line BL2 which is being preliminarily conducted receives a data signal having intermediate intensity between a maximum value and a minimum value of data signals which are applied to the signal lines.

Claim 5 (original): The method as set forth in claim 1, wherein the preliminary conduction of the BL2 is carried out during the normal conduction period of the BL1 within said one horizontal period.

Claim 6 (original): The method as set forth in claim 5, wherein the preliminary conduction of the BL2 is finished at the time when the normal conduction of the BL1 is finished within said one horizontal period, and normal conduction of the BL2 is carried out continuously thereafter.

Claim 7 (original): The method as set forth in claim 2, wherein the signal lines of the plurality of blocks are simultaneously conducted within said one horizontal period prior to the time the application of the data signal to the BL1 is finished.

Claim 8 (original): The method as set forth in claim 2, wherein, during the preliminary conduction of the BL2, the signal line BL2 which is being preliminarily conducted receives a data signal having intermediate intensity between a maximum value and a minimum value of data signals which are applied to the signal lines.

Claim 9 (original): The method as set forth in claim 2, wherein the preliminary conduction of the BL2 is carried out during the normal conduction period of the BL1 within said one horizontal period.

Claim 10 (original): The method as set forth in claim 9, wherein the preliminary conduction of the BL2 is finished at the time when the normal conduction of the BL1 is finished within said one horizontal period, and normal conduction of the BL2 is carried out continuously thereafter.

Claim 11 (withdrawn): A data transfer method in which scanning lines in a row direction and signal lines in a column direction are formed in a matrix pattern, and a data signal which corresponds to a position on the matrix is applied within one horizontal period to a signal line which corresponds to this position, the signal lines being divided into a plurality of blocks and being sequentially conducted for each line per block so as to transfer the data signal between a matrix section and a data transfer section, wherein:

when input data of one block, equivalent of n signal lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and are outputted to their corresponding signal lines, and

when the n sampling sections are divided into groups, and

when one of the blocks in which order of sampling the input data with respect to a single scanning line is second or after is BL2, and

when a group having a sampling section to which first sampling data Db1 of the block BL2 is inputted is GRa,

said method comprises the step of creating a blank sampling section for storing the sampling data Db1 in the group GRa, after the group GRa stores sampling data of a block in

which a sampling time is earlier than the block BL2 with respect to the single scanning line, and before, at the latest, the sampling data Db1 is inputted.

Claim 12 (withdrawn): The method as set forth in claim 11, wherein:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2,

each of said sampling sections has a plurality of systems for storing the sampling data, and

the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section in a group GR1, and

upon finishing the storage, another storage is started in another group with respect to next sampling data, and then the systems are switched in the group GR1 for the next storage to a system which does not currently store data, before storage of sampling data of the block BL2 is started in the group GR1.

Claim 13 (withdrawn): The method as set forth in claim 11, wherein when a group GR1 is one of the groups, sampling data stored in the group GR1 are outputted after they are stored at least in the group GR1, and while storing sampling data in another group.

Claim 14 (withdrawn): A data transfer method in which scanning lines in a row direction and signal lines in a column direction are formed in a matrix pattern, and a data signal which corresponds to a position on the matrix is applied within one horizontal period to a signal line which corresponds to this position, the signal lines being divided into a plurality of blocks and being sequentially conducted for each line per block so as to transfer the data signal between a matrix section and a data transfer section, said method comprising the step of,

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is

finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, said blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively:

starting the application of the data signal to the SL2 within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

Claim 15 (withdrawn): A data transfer method for an image display device having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and displaying an image according to a data signal by a pixel on the matrix, said method applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, and the data signal being transferred per block from a data transfer section to the pixel by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, said method comprising the step of,

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, said blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively:

starting the application of the data signal to the SL2 within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

Claim 16 (original): An image display device having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, said image display device displaying an image according to the data signal by a pixel on the matrix by transferring the data signal per block from a data transfer section to the pixel on the matrix by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, wherein:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, said blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively,

the data signal is transferred within one horizontal period from the data transfer section to the pixel on the matrix by inverting a polarity of a potential of the SL2 as preliminary conduction with respect to the reference voltage, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

Claim 17 (withdrawn): An image display device having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, said image display device displaying an image according to the data signal by a pixel on the matrix by transferring the data signal per block from a data transfer section to the pixel on the matrix by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, wherein:

when input data of one block, equivalent of n signal lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and outputted to their corresponding signal lines, and

when said n sampling sections are divided into groups, and

when one of the blocks in which order of sampling the input data with respect to a single scanning line is second or after is BL2, and

when a group having a sampling section to which first sampling data Db1 of the block BL2 is inputted is GRa,

the data signal is transferred from the data transfer section to the pixel on the matrix by creating a blank sampling section for storing the sampling data Db1 in the group GRa, after the group GRa stores sampling data of a block in which a sampling time is earlier than the block BL2 with respect to the single scanning line, and before, at the latest, the sampling data Db1 is inputted.

Claim 18 (withdrawn): An image display device having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, said image display device displaying an image according to the data signal by a pixel on the matrix by transferring the data signal per block from a data transfer section to the pixel on the matrix by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, wherein:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, said blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively,

the data signal is transferred from the data transfer section to the pixel on the matrix by starting the application of the data signal to the SL2 within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

Claim 19 (withdrawn): A signal line driving circuit having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, said signal line driving circuit transferring the data signal to a pixel on the matrix by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, wherein:

when input data of one block, equivalent of n signal lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and outputted to their corresponding signal lines, and

when the n sampling sections are divided into groups, and

when one of the blocks in which order of sampling the input data with respect to a single scanning line is second or after is BL2, and

when a group having a sampling section to which first sampling data Db1 of the block BL2 is inputted is GRa,

said signal line driving circuit generates a group control signal for specifying a timing of creating a blank sampling section for storing the sampling data Db1 in the group GRa, after the group GRa stores sampling data of a block in which a sampling time is earlier than the block BL2 with respect to the single scanning line, and before, at the latest, the sampling data Db1 is inputted.

Claim 20 (withdrawn): The signal line driving circuit as set forth in claim 19, wherein:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, said blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively,

the data signal is transferred within one horizontal period to the pixel on the matrix by inverting a polarity of a potential of the SL2 as preliminary conduction with respect to the reference voltage, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

Claim 21 (withdrawn): The signal line driving circuit as set forth in claim 19, wherein:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, said blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively,

the data signal is transferred within one horizontal period to the pixel on the matrix by starting the application of the data signal to the SL2, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

Claim 22 (withdrawn): The signal line driving circuit as set forth in claim 19, wherein:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and when a block for which the application of the data signal is finished later is BL2,

each of said sampling sections has a plurality of systems for storing the sampling data, and

the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section in a group GR1, and

upon finishing the storage, and before another storage is started in another group with respect to next sampling data, said signal line driving circuit generates a signal as the group control signal for specifying a timing of switching the systems in the group GR1 for the next storage to a system which does not currently store data, before storage of sampling data of the block BL2 is started in the group GR1.

Claim 23 (withdrawn): The signal line driving circuit as set forth in claim 19, wherein when a group GR1 is one of the groups, said signal line driving circuit generates a signal as the group control signal for specifying a timing of outputting the sampling data stored in the group GR1, after they are stored at least in the group GR1, and while storing sampling data in another group.

Claim 24 (original): An active-matrix substrate which includes a pixel switching element connected to each of a plurality of pixel electrodes, a plurality of scanning lines for driving the pixel switching element, a plurality of signal lines for applying a data signal to the pixel electrodes via the pixel switching element, and a signal input section for supplying the data signal to the signal lines so as to invert a polarity of a voltage of the signal lines, the signal lines being divided into blocks depending on a time the data signal is supplied in one horizontal period, said active-matrix substrate comprising:

a signal branching section for branching the data signal from the signal input section into respective blocks;

a signal line switching element for switching on or switching off supply of the data signal to respective signal lines from the signal branching section by being conducted or not conducted; and

a control wire, provided per block, for supplying a conduction signal to the signal line switching element, so as to switch conduction/non-conduction of the signal line switching element per block according to a supply time of the data signal, wherein:

with respect to at least one target block of at least two adjacent blocks, the data signal is applied to a control wire of an adjacent block earlier than a control wire of the target block within one horizontal period, and a signal line of the target block on a border between the adjacent blocks is preliminarily supplied with a preliminary polarity inverse signal for inverting a polarity of a voltage of the signal line of the target block, by an auxiliary signal line switching element which is controlled by being supplied with an auxiliary control signal from another auxiliary control wire which is different from the control wire of the target block, and which is different from the signal line switching element which is controlled by the control wire of the target block, prior to the time the supply of the data signal to the adjacent block is finished within one horizontal period.

Claim 25 (original): The active-matrix substrate as set forth in claim 24, wherein:

respective signal lines of the at least two adjacent blocks on the border between these blocks are supplied with the same preliminary polarity inverse signal via their respective auxiliary signal line switching elements, and

the supply of the preliminary polarity inverse signal is finished within one horizontal period before the supply of the data signal to the signal line which receives the data signal earlier is started.

Claim 26 (original): The active-matrix substrate as set forth in claim 24, wherein the auxiliary control wire is a control wire of another block which receives a conduction signal earlier than the control wire of the target block within one horizontal period.

Claim 27 (original): The active-matrix substrate as set forth in claim 26, wherein the auxiliary control wire is the control wire of the adjacent block which receives the conduction signal earlier than the control wire of the target block within one horizontal period.

Claim 28 (original): The active-matrix substrate as set forth in claim 24, wherein one of terminals of the auxiliary signal line switching element which is not connected to a signal line is electrically connected to a signal input section to which one of terminals of a signal line switching element which is controlled by the control wire of the target block, which is not connected to a signal line, is connected.

Claim 29 (original): The active-matrix substrate as set forth in claim 24, wherein one of terminals of the auxiliary signal line switching element which is not connected to a target signal line is electrically connected to a signal input section to which one of terminals of a signal line switching element which is connected to a signal line, in an adjacent block, adjacent to the target signal line, which is not connected to a signal line, is connected.

Claim 30 (original): The active-matrix substrate as set forth in claim 24, wherein one of terminals of the auxiliary signal line switching element which is not connected to a signal line is electrically connected to a signal input section to which one of terminals of a signal line switching element which supplies the data signal to a pixel which should display the same color as that of a pixel electrode which is connected to the signal line, and which is connected to another signal line closest to the signal line of the adjacent block, which is not connected to a signal line, is connected.

Claim 31 (original): The active-matrix substrate as set forth in claim 24, wherein a resistance of said signal line switching element is lower than that of the auxiliary signal line switching element during conduction.